Direct programming model
Data Parallel C++

Agenda

- What is Data Parallel C++?
- Anatomy of a DPC++ Application
- Memory model
- Compilation and Execution
- Device Selection
- Unified Shared Memory
- Intel® Compilers

What is Data Parallel C++?

The language is:

C++

+

SYCL* khronos.org/sycl/

+

Additional Features tinyurl.com/dpcpp-ext

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What is Data Parallel C++?

The implementation is:

Clang

+

LLVM https://github.com/intel/llvm

+

Runtime https://github.com/intel/compute-runtime

Code samples:

tinyurl.com/dpcpp-tests

tinyurl.com/oneapi-samples

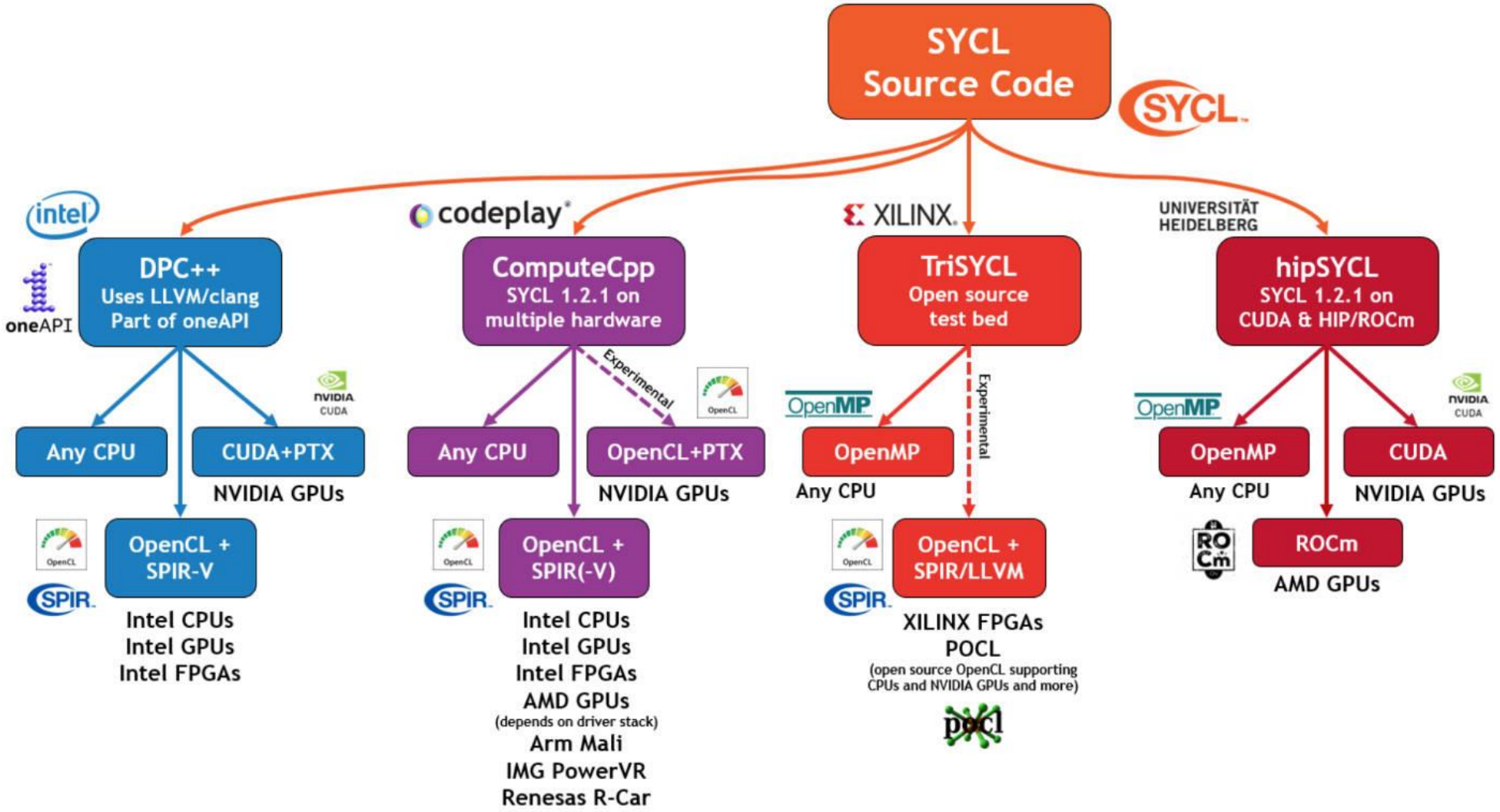
DPC++ Extensions

tinyurl.com/dpcpp-ext

tinyurl.com/sycl2020

Extension	Purpose	SYCL 2020
USM (Unified Shared Memory)	Pointer-based programming	✓
Sub-groups	Cross-lane operations	✓
Reductions	Efficient parallel primitives	✓
Work-group collectives	Efficient parallel primitives	✓
Pipes	Spatial data flow support	
Argument restrict	Optimization	
Optional lambda name for kernels	Simplification	✓
In-order queues	Simplification	✓
Class template argument deduction and simplification	Simplification	✓

SYCL implementation ecosystem



Anatomy of a DPC++ Application

```
#include <CL/sycl.hpp>
using namespace sycl;

int main() {
std::vector<float> A(1024), B(1024), C(1024);
// some data initialization
    {
      buffer bufA {A}, bufB {B}, bufC {C};
      queue q;
      q.submit([&](handler &h) {
          auto A = bufA.get_access(h, read_only);
          auto B = bufB.get_access(h, read_only);
          auto C = bufC.get_access(h, write_only);
          h.parallel_for(1024, [=](auto i){
              C[i] = A[i] + B[i];
          });
      });
    }
for (int i = 0; i < 1024; i++)
       std::cout << "C[" << i << "] = " << C[i] << std::endl;

}
```

Host code

Accelerator device code

Host code

Memory model

- SYCL abstractions for managing memory
  - Buffers
  - Images

SYCL* 1.2.1

- Powerful and elegantly expresses data dependences, but need to replace all pointers and arrays with buffers

- Unified Shared Memory (USM)

SYCL 2020

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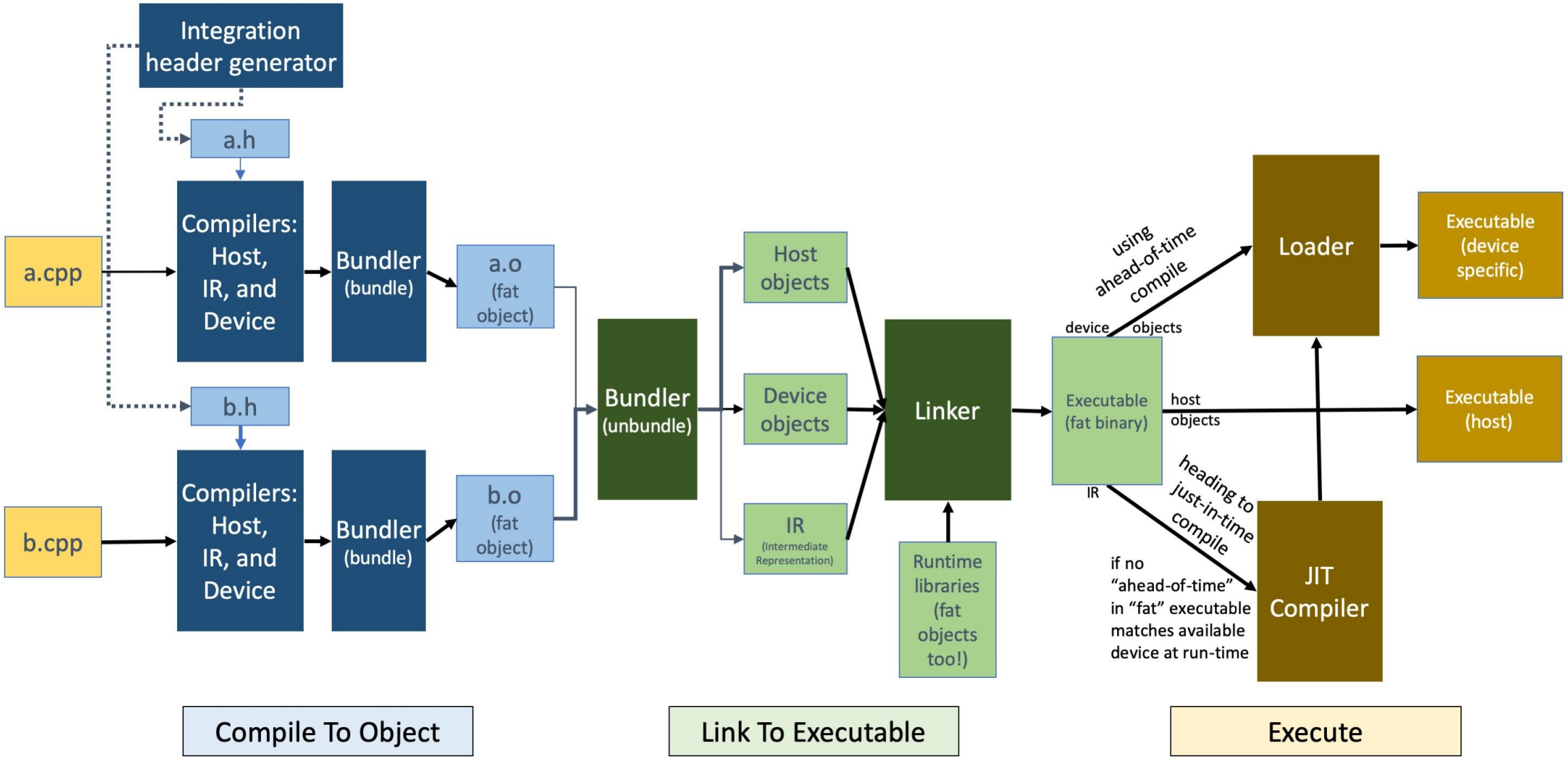
Buffers

```
std::vector<float> A(1024), B(1024), C(1024);
      {
        buffer bufA {A}, bufB {B}, bufC {C};
        queue q;
        q.submit([&](handler &h) {
            auto A = bufA.get_access(h, read_only);
            auto B = bufB.get_access(h, read_only);
            auto C = bufC.get_access(h, write_only);
            h.parallel_for(1024, [=](auto i){
                C[i] = A[i] + B[i];
            });
        });
      }
 for (int i = 0; i < 1024; i++)

        std::cout << "C[" << i << "] = " << C[i] << std::endl;

 }
```

SYCL 1.2.1 vs SYCL 2020

```
std::vector<float> A(1024), B(1024), C(1024);
{
  buffer<float> bufA {A.data(), A.size()};
  buffer<float> bufB{B.data(), B.size()};
  buffer<float> bufC {C.data(), C.size()};

  queue q;
  q.submit([&](handler &h) {
    auto A = bufA.get_access<access::mode::read>(h);
    auto B = bufB.get_access<access::mode::read>(h);
    auto C = bufC.get_access<access::mode::write>(h);
    h.parallel_for <class vector_add>(range<1>{1024}, [=](id<1> i){
                C[i] = A[i] + B[i];
            });
        });
      }
 for (int i = 0; i < 1024; i++)
        std::cout << "C[" << i << "] = " << C[i] << std::endl;
 }
```

DPC++ Compilation and Execution

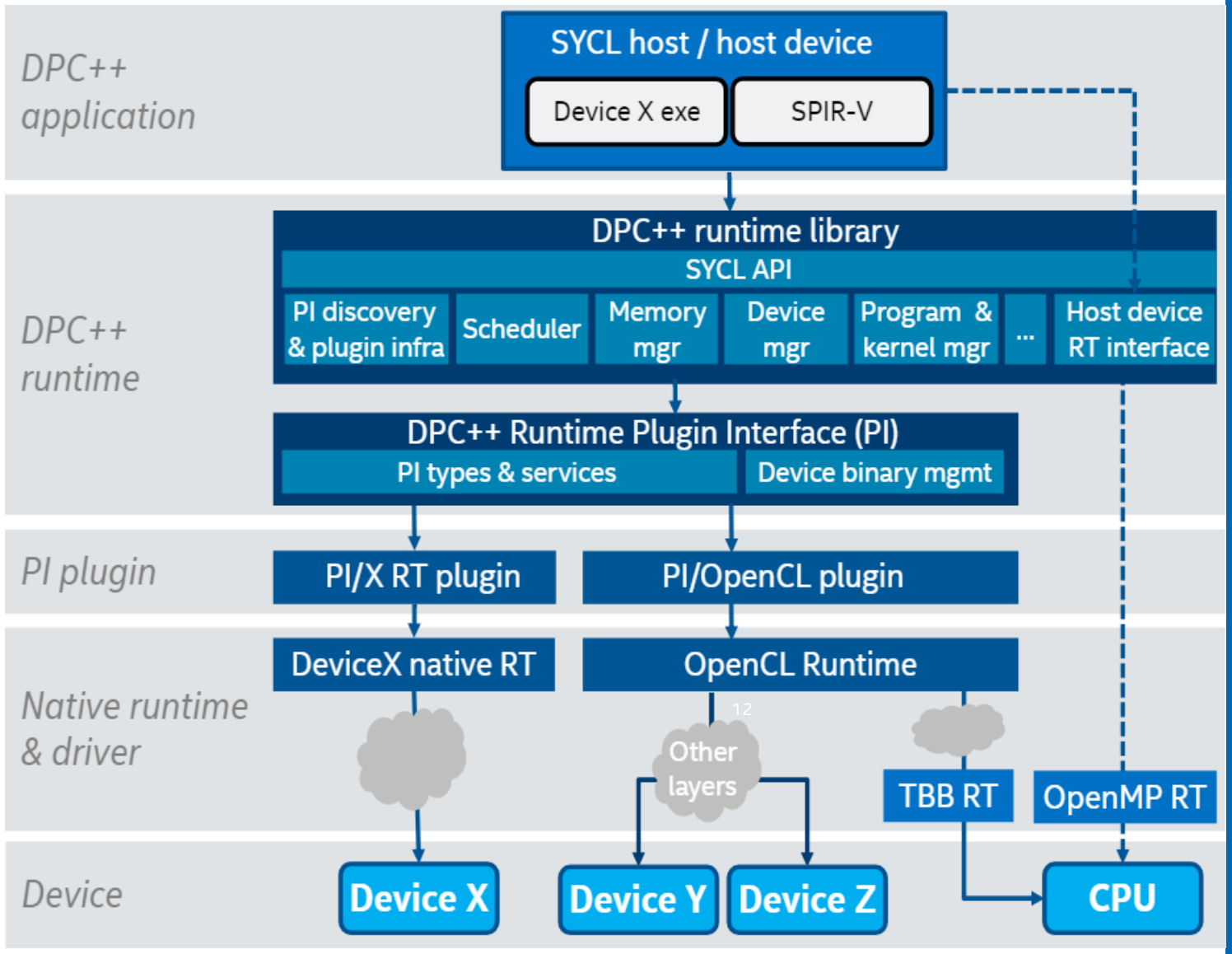


https://software.intel.com/en-us/oneapi-dpcpp-compiler-dev-guide-and-reference-ahead-of-time-compilation

DPC++ Execution Flow

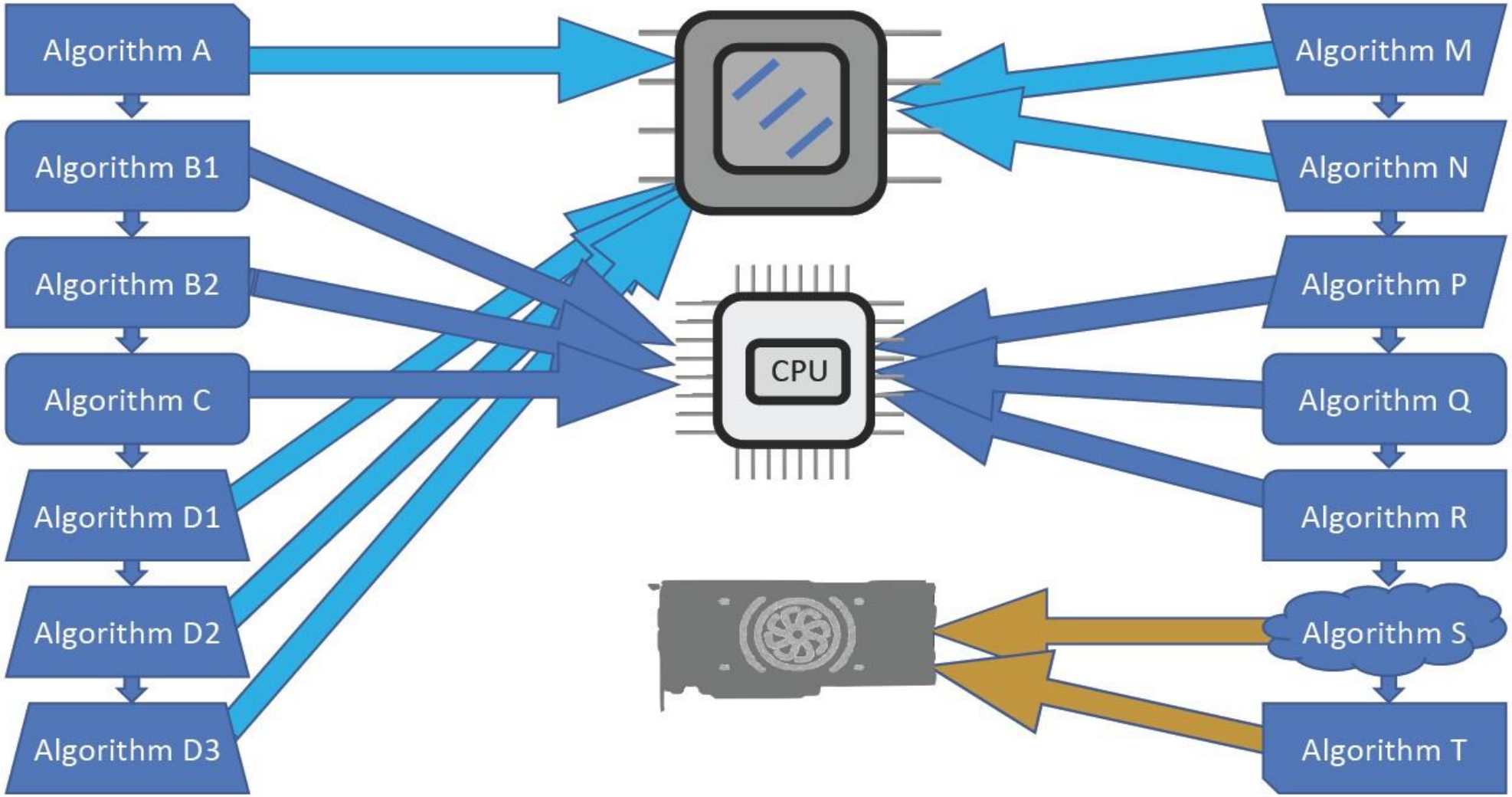
github.com/intel/llvm/tree/sycl/sycl/plugins

Controlled via SYCL_BE env var:
PI_OPENCL, PI_CUDA, PI_LEVEL0



More info: tinyurl.com/dpcpp-pi

DPC++ Device Selection



USM - Explicit Data Movement

```
queue q;
int hostArray[42];
int *deviceArray = (int*) malloc_device(42 * sizeof(int), q);

for (int i = 0; i < 42; i++) hostArray[i] = 42;
// copy hostArray to deviceArray
q.memcpy(deviceArray, &hostArray[0], 42 * sizeof(int));
q.wait();
q.submit([&](handler& h){
  h.parallel_for(42, [=](auto ID) {
    deviceArray[ID]++;
  });
});
q.wait();
// copy deviceArray back to hostArray
q.memcpy(&hostArray[0], deviceArray, 42 * sizeof(int));
q.wait();
free(deviceArray, q);
```

USM – Implicit Data Movement

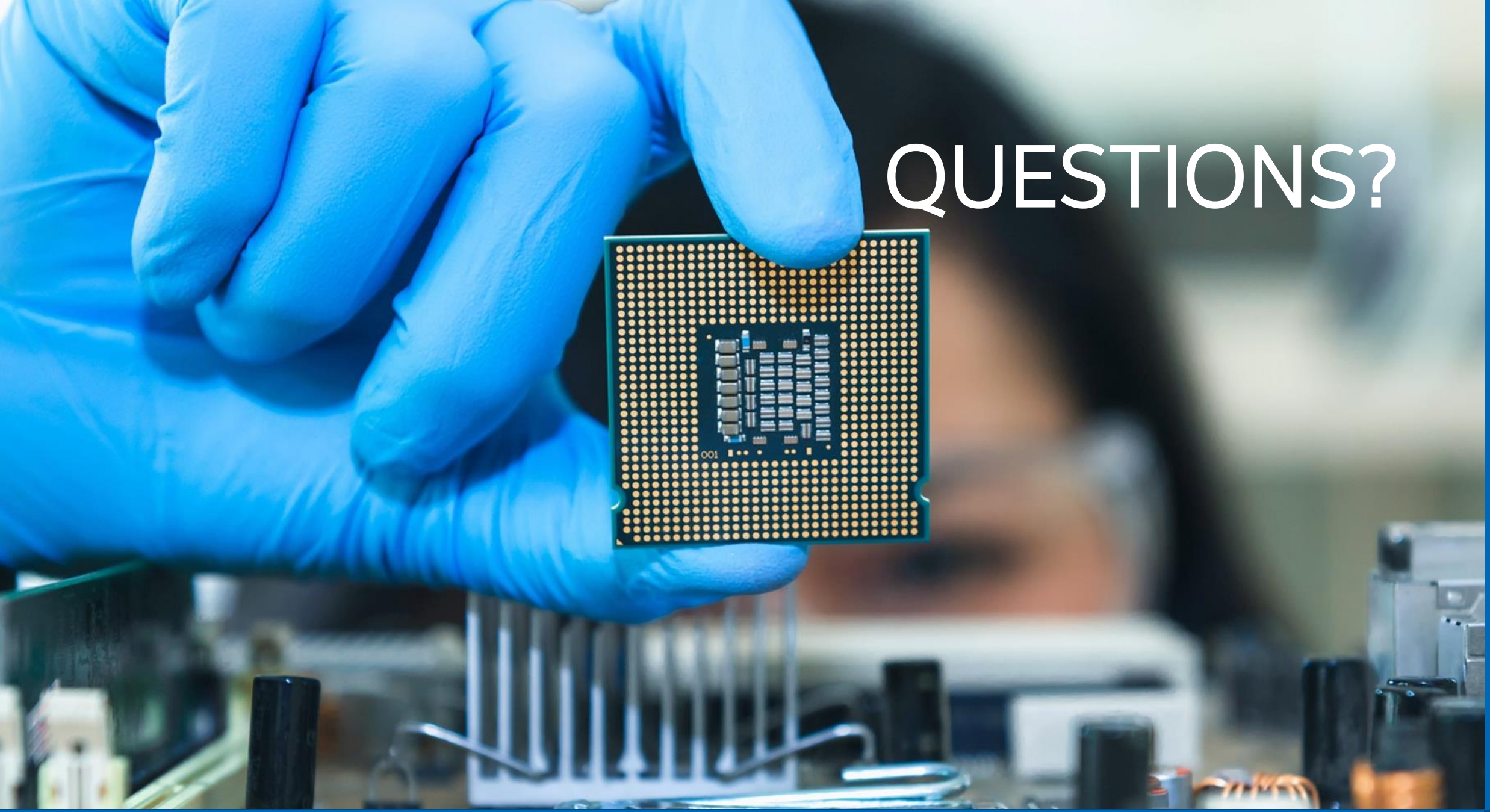
```
queue q;
int *hostArray = (int*) malloc_host(42 * sizeof(int), q);
int *sharedArray = (int*) malloc_shared(42 * sizeof(int), q);

for (int i = 0; i < 42; i++) hostArray[i] = 1234;
q.submit([&](handler& h){
  h.parallel_for(42, [=](auto ID) {
    // access sharedArray and hostArray on device
    sharedArray[ID] = hostArray[ID] + 1;
  });
});
q.wait();
for (int i = 0; i < 42; i++) hostArray[i] = sharedArray[i];
free(sharedArray, q);
free(hostArray, q);
```

Intel® Compilers

Intel Compiler	Target	OpenMP Support	OpenMP Offload Support	Included in oneAPI Toolkit
Intel® C++ Compiler, IL0 (icc)	CPU	Yes	No	HPC
Intel® oneAPI DPC++/C++ Compiler (dpcpp)	CPU, GPU, FPGA*	No	No	Base
Intel® oneAPI DPC++/C++ Compiler (ICX)	CPU GPU*	Yes	Yes	Base and HPC
Intel® Fortran Compiler, IL0 (ifort)	CPU	Yes	No	HPC
Intel® Fortran Compiler (ifx)	CPU, GPU*	Yes	Yes	HPC

Cross Compiler Binary Compatible and Linkable!

*Intel® Platforms
**PSXE 2020 Production+oneAPI HPC Toolkit(BETA)
*** IFX will remain in BETA in 2021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